a host device;

a first media access interface having a first media access architecture for processing the digital signal to provide information to the host device;

a second media access interface having a second media access architecture for processing the digital signal to provide information to the host device;

wherein the first media access architecture is primarily independent from the host device; and

wherein the second media access architecture is primarily dependent on the host device.

2. The system of claim 1 wherein the first media access interface and the frequency converter are housed on a first chipset; and

wherein the second media access interface is housed on a second chipset.

3. The system of claim 1 wherein the first media access interface, the frequency converter, and the transceiver are housed a first chipset; and

wherein the second media access interface is housed on a second chipset.

4. The system as in claim 2, wherein the first media access architecture comprises a data store having host device data corresponding to the properties of host device.

5. The system as in claim 4, wherein the host device data represents the bus size of the host device.

6. The system as in claim 5, wherein the data store comprises a plurality of double synchronizing flip flops capable of operating asynchrously with the first media access interface.

7. The system as in claim 5, wherein the data store is implemented using software.

* * * * *